**LESSON PLAN**

**Branch**: III ECE ‘A'**Semester**: II **Subject** :VLSI

**Acadamicyear:2017-18faculty :M chaitanya Kumar**

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| Period | Date (Tentative) | Topic | Unit No. | Teaching Methodology | Remarks | Corrective Action upon Review |
|  |  | **Introduction** | I |  |  |  |
|  | 21-11-17 | Introduction to IC Technology | I | Black Board |  |  |
|  | 22-11-17 | The IC era, MOS and related VLSI technology and basic MOS transistors. | I | B.B |  |  |
| 3-6 | 23-11-17 to 29-11-17 | IC production process | I | B.B |  |  |
| 7-11 | 2-12-17 to 7-12-17 | MOS and CMOS fabrication process. | I | PPT |  |  |
| 12 | 9-12-17 | Bi-CMOS technology | I | PPT |  |  |
| 13 | 12-12-17 | Comparison between CMOS and bipolar technologies. | I | PPT |  |  |
|  |  | **Basic electrical properties of MOS and Bi-CMOS circuits** | II |  |  |  |
| 14 | 13-12-17 | Ids – Vds relationship | II | B.B |  |  |
| 15 | 14-12-17 | Aspects of MOS transistor: threshold voltage, trans-conductance, output conductance and figure of merit. | II | B.B |  |  |
| 16 | 16-12-17 | Pass transistor, MOS inverter | II | B.B |  |  |
| 17 | 19-12-17 | Determination of pull-up to pull-down ratio of NMOS. | II | B.B |  |  |
| 18 | 20-12-17 | NMOS inverter driven by another NMOS inverter and driven through one or more pass transistors | II | B.B |  |  |
| 19 | 2-1-18 | Alternative forms of pull-up | II | B.B |  |  |
| 20 | 3-1-18 | CMOS inverter | II | B.B |  |  |
| 21 | 4-1-18 | MOS transistor circuit model | II | B.B |  |  |
| 22 | 6-1-18 | Bi-CMOS inverter and latch-up in CMOS circuits. | II | B.B |  |  |
|  |  | **VLSI Circuit design process& Scaling of MOS circuits** | III |  |  |  |
| 23 | 9-1-18 | VLSI design flow, | III | B.B |  |  |
| 24 | 10-1-18 | layers of abstraction | III |  |  |  |
| 25, 26,27 | 11-1-18 to 18-1-18 | stick diagrams | III | B.B |  |  |
| 28 | 20-1-18 | Design rules for wires | III | PPT |  |  |
| 29 | 23-1-18 | contacts and transistor | III | PPT |  |  |
| 30 | 27-1-18 | layout diagrams for NMOS &CMOS inverters and gates. | III | PPT |  |  |
| 31 | 30-1-18 | Scaling models, | III | B.B |  |  |
| 32 | 1-2-18 | Scaling factors | III | B.B |  |  |
| 33 | 3-2-18 | Device parameters | III | B.B |  |  |
| 34 | 6-2-18 | Limitations of scaling. | III | B.B |  |  |
|  |  | **Gate Level Design& Basic circuit concepts** | IV |  |  |  |
| 35 | 13-2-18 | Logic gates and other complex gates | IV |  |  |  |
| 36 | 14-2-18 | Switch logic | IV | B.B |  |  |
| 37,38 | 15-2-18, 17-2-18 | Alternate gate circuits. | IV | B.B |  |  |
| 39 | 20-2-18 | Sheet resistance(Rs) and its concept to MOS. | IV | B.B |  |  |
| 40 | 21-2-18 | Area capacitance | IV | B.B |  |  |
| 41 | 22-2-18 | calculations | IV | B.B |  |  |
| 42 | 24-2-18 | delays | IV | B.B |  |  |
| 43 | 27-2-18 | driving large capacitive load | IV | B.B |  |  |
| 44 | 28-2-18 | wiring capacitances | IV | B.B |  |  |
| 45 | 1-3-18 | fan-in and fan-outs and choice of layers. | IV | B.B |  |  |
| 46 | 3-3-18 | Subsystem Design, Shifters adders, | IV | B.B |  |  |
| 47 | 5-3-18 | ALUs | IV | B.B |  |  |
| 48 | 6-3-18 | multipliers | IV | B.B |  |  |
| 49 | 7-3-18 | Parity generators. | IV | B.B |  |  |
|  |  | **Design Methods& CMOS Testing** | V |  |  |  |
| 50 | 8-3-18 | Design-capturetools | V | B.B |  |  |
| 51 | 10-3-18 | Design- verification tools. | V | B.B |  |  |
| 52 | 13-3-18 | Need for CMOS testing | V | B.B |  |  |
| 53 | 14-3-18 | Manufacturing test principles | V | B.B |  |  |
| 54 | 15-3-18 | Design strategies for test. | V | B.B |  |  |
| 55 | 17-3-18 | Chip level test techniques | V | B.B |  |  |
| 56 | 20-3-18 | System level test techniques. | V | B.B |  |  |
| 57 | 21-3-18 | Revision | V | B.B |  |  |

**Text books:**

1. Essentials of VLSI circuits and systems – KamranEshraghian, EshraghianDougles and A. Pucknell, PHI, 2005.
2. Principles of CMOS VLSI Design – Weste and Eshraghian, Pearson Education, 1999.

**Reference books:**

1. VLSI Design – Debaprasad Das, Oxford university press, 2010.
2. VLSI Design – A.Albert Raj and T.Latha, PHI Learing private limited 2010.
3. ASIC design - Smith.